What is claimed is:

1. A data communications system, which comprises:

a first node for transmitting an output digital signal to a second node through a transmission line and receiving an input digital signal from the second node through a reception line, wherein the first node having a transmission port for transmitting the output digital signal and a reception port for receiving the input digital signal; and

a signal processing amplification block for compensating an attenuation of the input digital signal and preventing a crosstalk between the transmission line and the reception line, wherein an input port of the signal processing amplification block is connected to the second node through the reception line and an output port of the signal processing amplification block is connected to the reception port.

2. The data communications system of claim 1, wherein the signal processing amplification block includes:

a limiting circuit for clamping the input digital signal to make it fall within a predetermined range;

a phase compensation amplification circuit for amplifying the clamped digital signal; and

a regulating circuit for rectifying a branch signal and generating a control signal to alter an amplification

gain of the phase compensation amplification circuit, based on a length of the reception/transmission line and a capacity of the branch signal, the branch signal being a portion of the output digital signal, a portion of the input digital signal or a noise signal.

3. The data communications system of claim 2, wherein the limiting circuit has:

a circuit for matching an impedance of the input digital signal with an impedance of the reception line and rejecting a common mode component of the input digital signal; and

a circuit for rejecting a reverse recovery current occurred in operation of the limiting circuit.

4. The data communications system of claim 2, wherein the phase compensation amplification circuit has:

a circuit for controlling an amplification gain of the phase compensation amplification circuits in proportion to a frequency of the clamped digital signal, and preventing the amplification gain from being out of a predetermined range;

a differential amplifier circuit for amplifying the clamped digital signal; and

a circuit for clamping the amplified digital signal from the differential amplifier circuit to make it fall within a predetermined range.

5. The data communications system of claim 2, wherein an input end of the regulating circuit is linked to the transmission port or the transmission line at a position close to the transmission port, to thereby rectify the portion of the output digital signal or the noise signal and generate the control signal.

6. The data communications system of claim 2, wherein an input end of the regulating circuit is linked to the reception line at a position close to the input port of the signal processing amplification block, to thereby rectify the portion of the input digital signal or the noise signal and generate the control signal.

7. The data communications system of claim 1, wherein the signal processing amplification block includes:

a first limiting circuit for clamping the input digital signal to make it fall within a predetermined range;

a second limiting circuit for generating an output signal under a control of a control signal from a control circuit;

the control circuit for generating the control signal to activate the second limiting circuit to pass the clamped digital signal as the output signal based on a length of the reception/transmission line and a capacity of a branch

signal, the branch signal being a portion of the output digital signal, a portion of the input digital signal or a noise signal;

a signal combination circuit for superposing the output signal from the second limiting circuit on the clamped digital signal from the first limiting circuit to generate a superposed signal; and

a phase compensation amplification circuit for amplifying the superposed signal.

8. The data communications system of claim 7, wherein the first limiting circuit has:

a circuit for matching an impedance of the input digital signal with an impedance of the reception line and rejecting a common mode component of the input digital signal; and

a circuit for rejecting a reverse recovery current occurred in operation of the first limiting circuit.

9. The data communications system of claim 7, wherein the signal combination circuit has a regulating unit for adjusting an amplification gain for the output signal from the second limiting circuit in proportion to a frequency of the output signal.

10. The data communications system of claim 7, wherein the phase compensation amplification circuit has:

a circuit for controlling an amplification gain of the phase compensation amplification circuit in proportion to a frequency of the superposed signal, and preventing the amplification gain from being out of a predetermined range;

a differential amplifier circuit for amplifying the superposed signal; and

a circuit for clamping the superposed signal from the differential amplifier circuit to make it fall within a predetermined range.

11. The data communications system of claim 1, which further comprises an output signal amplification circuit for compensating the attenuation of the output digital signal, wherein an input port of the output signal amplification circuit is connected to the first node through the transmission line and an output port of the output signal amplification circuit is connected to the second node.

12. The data communications system of claim 11, wherein the output signal amplification circuit matches an output impedance thereof with an impedance of the transmission line.

13. A data communications system, which comprises:

a first node for transmitting an output digital signal

to a second node through a transmission line and receiving an input digital signal from the second node through a reception line, wherein the first node having a transmission port for transmitting the output digital signal and a reception port for receiving the input digital signal;

an amplification device for amplifying the input digital signal, wherein an input port of the amplification device is connected to the second node through the reception line and an output port of the amplification device is connected to the reception port; and

a regulating block, coupled to the amplification device, for generating a control signal to alter an amplification gain of the amplification device, to thereby prevent a crosstalk between the transmission line and the reception line.

14. The data communications system of claim 13, wherein the regulating block includes:

a circuit for rectifying the portion of the output digital signal or the noise signal; and

a circuit for generating the control signal based on a capacity of the rectified signal to transmit the control signal to the amplification device.

15. The data communications system of claim 14, wherein an input end of the regulation block is linked to the

transmission port or the transmission line at a position close to the transmission port.

16. The data communications system of claim 13, wherein the regulating block includes:

a circuit for rectifying the portion of the input digital signal or the noise signal; and

a circuit for generating the control signal based on a capacity of the rectified signal to transmit the control signal to the amplification device.

17. The data communications system of claim 16, wherein an input end of the regulating block is linked to the reception line at a position close to the input port of the amplification device.